REMARKS

Favorable consideration and allowance of the claims of the present application are respectfully requested.

In the present Official Action, Claims 23-25 were rejected under 35 U.S.C. §112, 2nd paragraph, as allegedly failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner particularly objects to the use of the term "can be" recited in the claims. Applicants in response have amended the claim to remove the alleged indefinite language.

Further in the Official Action, the Examiner had rejected Claims 1, 2, 7, 8, 13 and 17-19 and 23-25 under 35 U.S.C. §102(e) as allegedly anticipated by Nadeau-Dostie et al. (US Patent Pub. No. 2005/0047229) ("Nadeau-Dostie").

Further, Claims 3-6, 9-12, 14-16 and 20-22 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Nadeau-Dostie in further view of US Patent No. 6,978,402 to Hirabayashi ("Hirabayashi ").

With respect to the rejection of Claims 1, 2, 7, 8, 13 and 17-19 and 23-25 under 35 U.S.C. §102(e) as allegedly anticipated by Nadeau-Dostie, applicants respectfully traverse in view of the amendments made herein to Claims 1, 7, 13 and 17 that distinguish the present invention over Nadeau-Dostie.

Particularly, the important feature of the invention is the performance of the BIST testing, performed under control of the high speed multiplied clock which is an asynchronous multiple of an external clock (i.e., a multiple of an external ATE (tester) clock speed) that generates a fail map data for capture by a diagnostic register device and while the BIST testing is paused upon recognition of a fail of the embedded memory system, automatically reconfiguring the same

diagnostic register device to read bit fail data out directly from the diagnostic register device to the tester in a serial fashion under control of the external clock of the tester; and then resuming the BIST testing with the high speed multiplied clock from the point at which it was paused.

Respectfully, no new matter is being entered, for example, as the recitation directed to the high speed multiplied clock being an asynchronous multiple of an external clock, is set forth in paragraph [0072] of the present specification (for instance).

Thus, the present invention, as now claimed in amended Claims 1, 7, 13 and 17 has further distinguished over the Nadeau-Dostie references and applicants further submit the following:

Fundamentally, the present invention application's purpose is different than Nadeau-Dostie. The differing objectives make it difficult for Nadeau-Dostie to be read in a manner that anticipates the present invention. Nadeau-Dostie focuses on fail compression improvements, while the present invention focuses on BIST-tester interaction during diagnostic data collection.

Thus, with respect to the method Claims 1 and 7, these claims significantly differ from Nadeau-Dostie as the method of operation in the present invention is significantly less complex than Nadeau-Dostie, while providing more detailed diagnostic information. Basically, Nadeau-Dostie concentrates on methods for fail compression, while the present invention focuses on efficient BIST-tester interaction methods during diagnostic data collection.

That is, with respect to the differences in the methods of operation, the present invention implements a method outlined in Fig. 7 of the present specification that highlights a streamlined BIST-Tester interface. This timing diagram of Fig. 7 describes this sequence: Test -> Fail Discovered / diagnostic register device captures fail data (CFD=1) -> Test Paused / Tester Alerted (FAIL NET=1) -> Tester Acknowledges Fail / diagnostic register device reconfigured

for serial transfer (TII = 1) -> serial unload occurs (SHIFT NET = 1) -> Test resumes (SHIFT NET = 0). This sequence is clearly described in the present specification at paragraphs [0040]-[0044] (referencing the circuit diagrams) and [0051]- [0056] (referencing the timing diagram). Respectfully, Claims 1 and 7 clearly describe this method. However, for further clarity, Claims 1 and 7 are being further amended herein to highlight that all diagnostic fails data are captured in this method (see present specification at paragraph [0030]) and that the single register is automatically reconfigured using a simple BIST-Tester interface. Thus, Claim 1 is amended to set forth: reconfiguring said diagnostic register device from a data capture mode controlled by the high speed multiplied clock to a serial transfer mode controlled by the tester clock; and using the external clock of the tester to read bit fail data out from said diagnostic register device to the tester before resuming the BIST testing with the high speed multiplied clock from the point at which it was paused.

Nadeau-Dostie, on the other hand, describes a complex method shown in Fig. 3 (of Nadeau-Dostie) that relies heavily on the BIST test sequence and the amount of fails discovered during each pass in order to produce an accurate failure summary (in Figure 3, steps 36-52 are completely unnecessary in the method of the present invention because a failure summary is not needed). Nadeau-Dostie focuses on "testing each memory location of said column or row according to a memory test algorithm"... and..."transferring said failure summary from said circuit". They describe the compressed information in Figure 4 (essentially first and last fail detected and an overflow if more than two fails are found). The key is that this information is a simple summary of the total number of fails seen. Nowhere do they claim an ability to capture all fails on a row or column element in one test pass.

In further distinction, Nadeau-Dostie must test and capture fail data and transmit a summary of the failure data (capturing and transferring the raw data would take far too much area for their method). This reduced detail is enough for some analysis, but as clearly stated in paragraph 49 to gather more detail "memory test can be repeated and focus on portions of the memory". However, Nadeau-Dostie's complicated method is an attempt to balance circuit area, diagnostic information and test time, by focusing on how failure data compression works. They require repeated tests in order to obtain truly accurate diagnostic information when many fails are present.

The method of the present invention rather, allows for all diagnostic fails data (every single fail regardless of the number of fails) to be captured and transferred to the tester in a single test pass using an efficient interface.

Further, with respect to the independent structure Claims 13 and 17, these claims, as now amended, significantly differ from Nadeau-Dostie in that they set forth the use of one single register (diagnostic register device in Claim 13 and bit fail map data register in Claim 17) that captures diagnostic information. This same register is used to transfer the data off chip. This diagnostic register device is automatically reconfigured to handle both modes of operation (as set forth in amended Claims 13 and 17. Nadeau-Dostie, in contrast, relies on two distinct registers. Nadeau-Dostie provides no means for combining these two registers.

That is, with respect to the structural differences, the present invention uses one main register that serves a dual purpose: capturing failing memory information at a high-speed clock, and transferring the failing memory data off chip at a slower clock speed. Figure 1 of the present application depicts an FM Register 11 that captures diagnostic data on its "D" input. This same FM Register 11 is used to serially transfer data to the tester through the Mux 15. Only one

register is used to both capture the diagnostic data and transfer it to the tester. This one FM Register 11 is automatically reconfigured when a fail is detected to transition from data capture to data transfer operation. Thus, the present Claims 13 and 17 further set forth a means implementing logic for automatically reconfiguring said diagnostic register device from a data capture mode controlled by the high speed multiplied clock to a serial transfer mode controlled by the tester clock. Claim 13, in addition, has been amended to set forth that the circuit uses the tester clock to read bit fail data out to the tester from said diagnostic register device.

Further, Claim 17 more specifically has been amended to set forth a bit fail map data register having diagnostic latches used to store data on failing memory locations for the generation of a bit fail map in a data capture mode controlled by a high speed multiplied clock which is an asynchronous multiple of the tester clock and, that a second control latch ... enables a shift out of the data on failing memory locations from the bit fail map data register in a serial transfer mode controlled by the tester clock for the generation of a bit fail map.

As mentioned, Nadeau-Dostie, to the contrary, uses two main registers. Particularly, Figure 8 in Nadeau-Dostie shows a Failure Address Register 176 that captures failing data information. This data is copied to a second Transfer Register 180 for transfer to the tester. Two registers are thus required to capture the failing data and transfer it off chip. Nadeau-Dostie (in its structural claim) describe a "means for transferring said failure summary from said circuit via a circuit output under control of a second clock while testing the next column or row" (Claim 41 of Nadeau-Dostie). Claim 42 elaborates on the structure with "said means for generating a failure summary including a transfer register for storing failure summary data". These claims, together with the specification, describe a first circuit that generates a failure summary using one clock and a second circuit that transfers the data off-chip using a second clock.

In sum, the purpose of Nadeau-Dostie is different than the present invention. Nadeau-Dostie describes attempting to "compress failure information that needs to be transferred without sacrificing the ability of extracting relevant failure information" in paragraph [0012] of Nadeau-Dostie. That is, Nadeau-Dostie focuses on failure compression, ignoring increases in test time and circuit area. Nadeau-Dostie is simply looking for a method that yields acceptable compression of failure information with the ability to repeat testing to gain more detailed fail info without greatly increasing area/test time. Nadeau-Dostie, with their focus on failure compression do not anticipate a need to use a single register for collecting data. The number of registers is irrelevant when seeking an optimum compression strategy- and the teachings of Nadeau-Dostie just does not describe/claim in any detail either how the data is transferred to the tester, how the tester interfaces with the BIST circuitry to control the transfer, or how BIST testing can continue afterwards. Nadeau-Dostie's goal is failure compression without too much loss of accuracy (see paragraph [0012] of Nadeau-Dostie).

The present invention claim clearly describes attempting to "accurately bit fail map...by stopping the BIST test circuitry at a point when a fail is encountered...shifting the bit fail data off the chip using the low-speed ATE tester clock, and then resuming the test by again running the BIST using the high-speed internal clock". The invention's ability to pause and shift out detailed (un-summarized) fail data and resume testing reduces test time, because the memory test does not need to be repeated if many (more than 3) fails occur. This pause/resume is clearly defined in amended Claim 1 with no mention of summarizing fail information. The difference here is that the purpose of the present invention focuses on automatically stopping/starting BIST test to obtain bit fail map information and as such focuses on circuits/methods that enable this feature with the least overhead in test time/area possible, and how this method works with the tester.

Nadeau-Dostie purpose is to claim advances in fail data compression and NOT for the purpose of improving the interaction between the BIST and tester during fail data collection.

In view of the foregoing, the applicants submit that amended Claims 1, 7, 13, and 17 set forth novel subject matter as each element is neither taught nor described by Nadeau-Dostie.

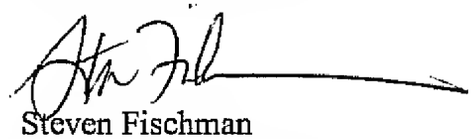
With respect to the rejection of Claims 3-6, 9-12, 14-16 and 20-22 under 35 U.S.C. §103(a) as allegedly unpatentable over Nadeau-Dostie in further view of Hirabayashi Applicants respectfully submit that Hirabayashi does not make up the deficiencies of Nadeau-Dostie. Hirabayashi simply describes how to generate multiplied clocks and select between them. The key to the present invention is implementing a circuit/method that allows a tester to interact with the test circuitry across an asynchronous interface to recognize fail data is available, stop test, switch clocks and synchronously unload the data without requiring a complicated data synchronizing state machine, or an extra transfer register, as required by the teachings of Nadeau-Dostie.

Thus, in view of the foregoing, the Examiner is respectfully requested to withdraw the rejections of Claims 1, 2, 7, 8, 13 and 17-19 and 23-25 under 35 U.S.C. §102(e) and, additionally, withdraw the rejections of Claims 3-6, 9-12, 14-16 and 20-22 under 35 U.S.C. §103(a).

In view of the foregoing, this application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a

telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,



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